

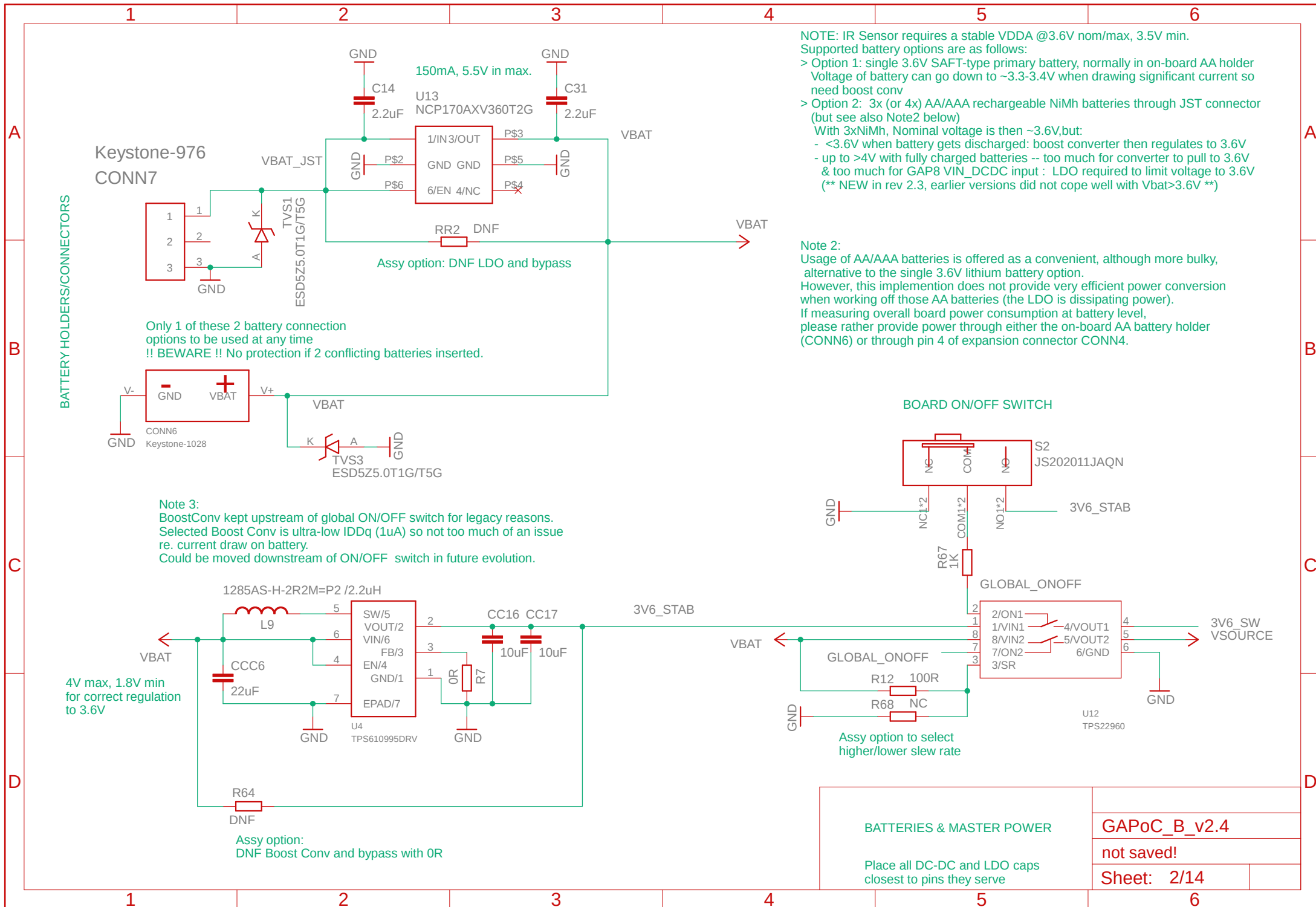
NINA_CTS/RT/TX connections to GAPMod:
 - not available with GAPMod1.2 (DNF resistors)
 - provision implementation of h/w flow control if using a GAPMod2.1 - in which case the pins are available as GPIO/Timer for flow ctrl. See Gwt AN003.

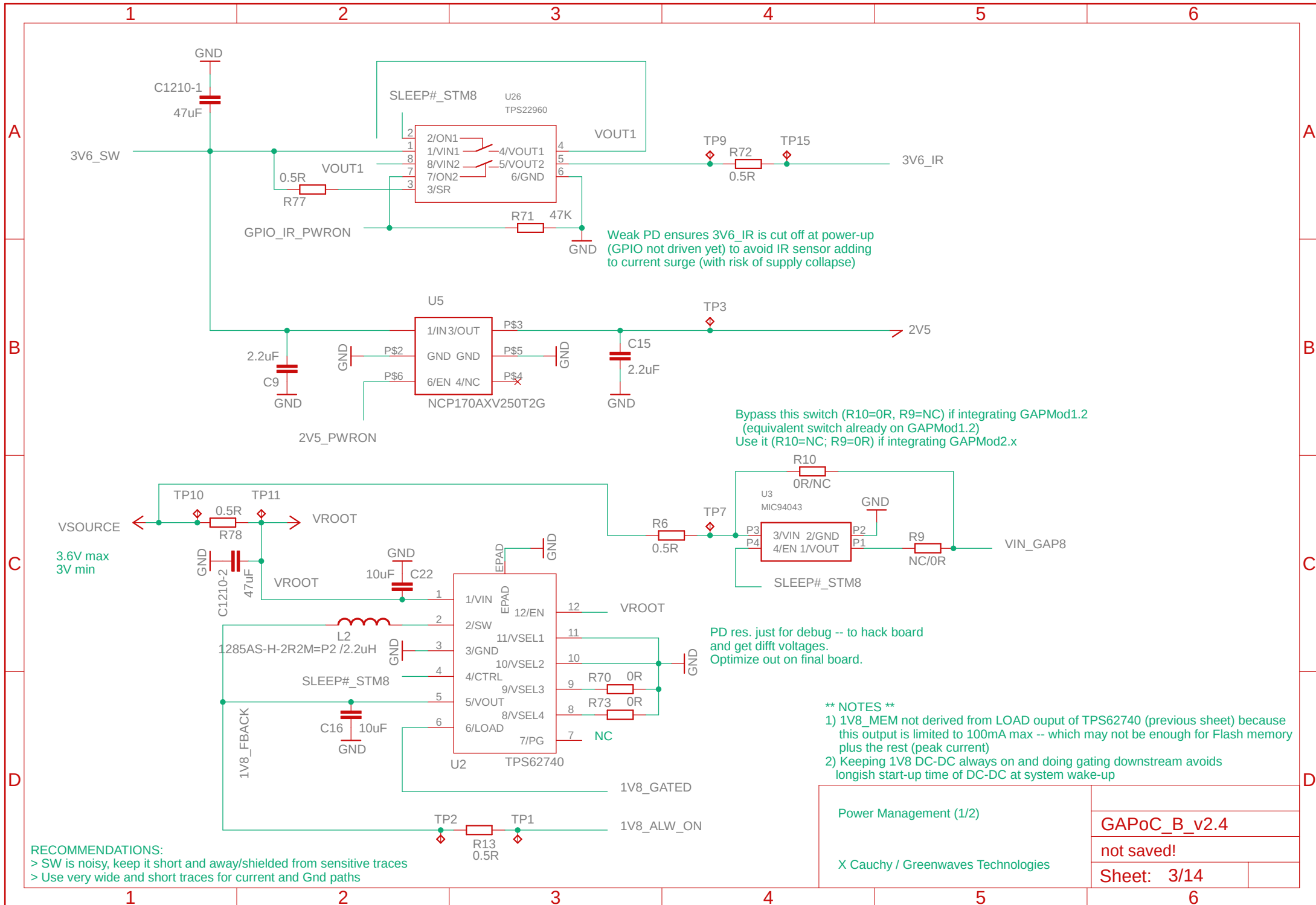
GAPMod (GAP8) Connections
 X Cauchy / Greenwaves Technologies

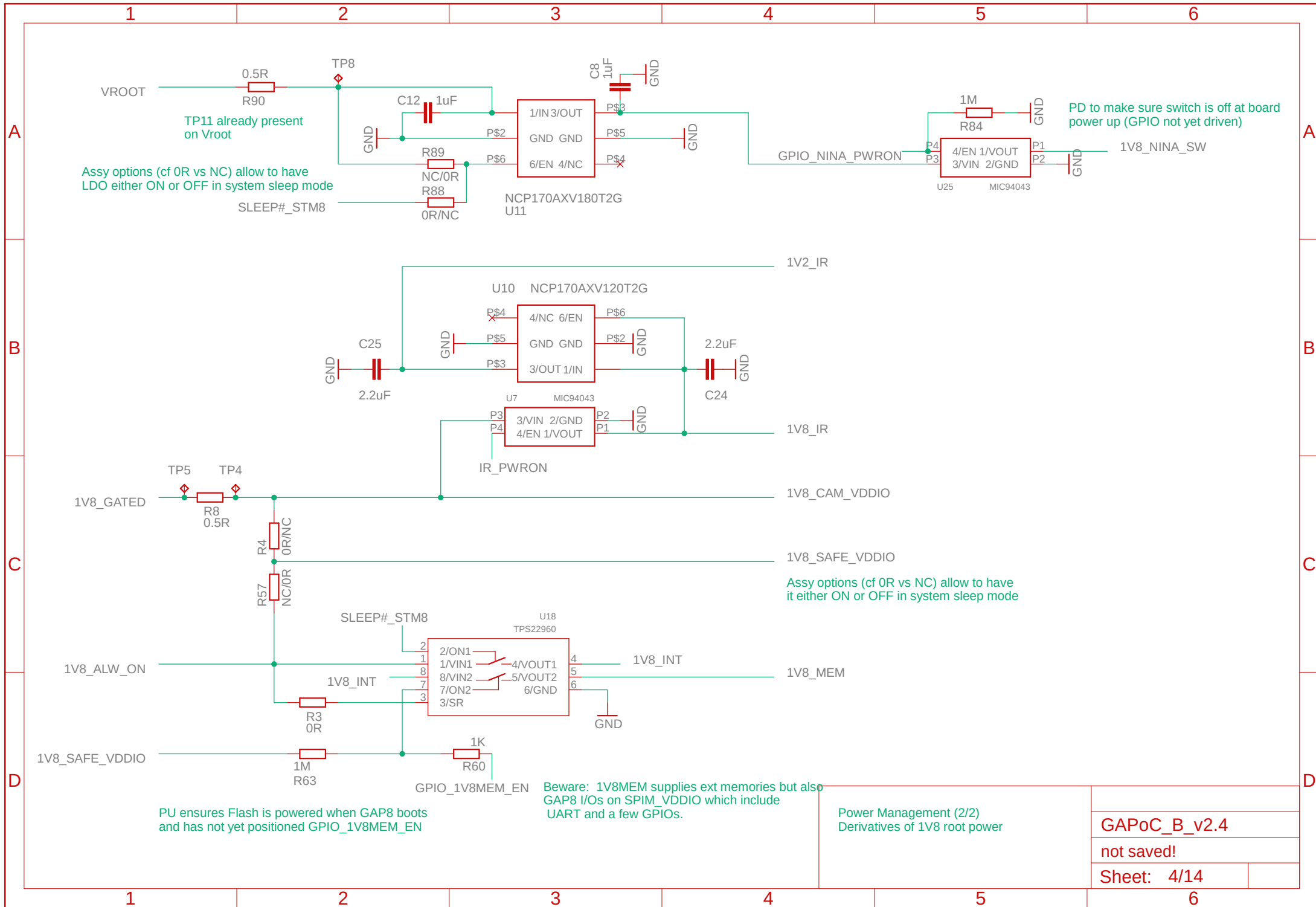
GAPoC_B_v2.4

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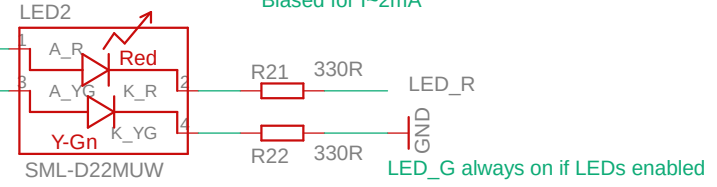




NOTE on LEDs :
 I/Os controlling LEDs are 0V-1V8 while Vf of LED is ~1.8v-2V.
 In this design, applying 2.5V on anode and controlling cathode from I/O, so that:
 - LED ON when I/Os is 0V.
 - LED Off when I/O driven to either Logic1 (1.8V) or (better) High-Z
 Some small current might still circulate in OFF mode, but not enough to light LED (or perhaps, if applying 1 Logic1 rather than High-Z, extremely dim).
 Not an issue from power perspective as only used in debug mode (2V5 can be switched off in normal mode)
 [Also applies to other 2V5-powered LEDs used in this design]

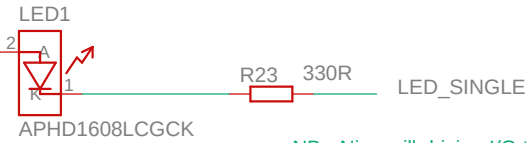
Using diff LED color scheme vs. Nina spec

Biased for I~2mA

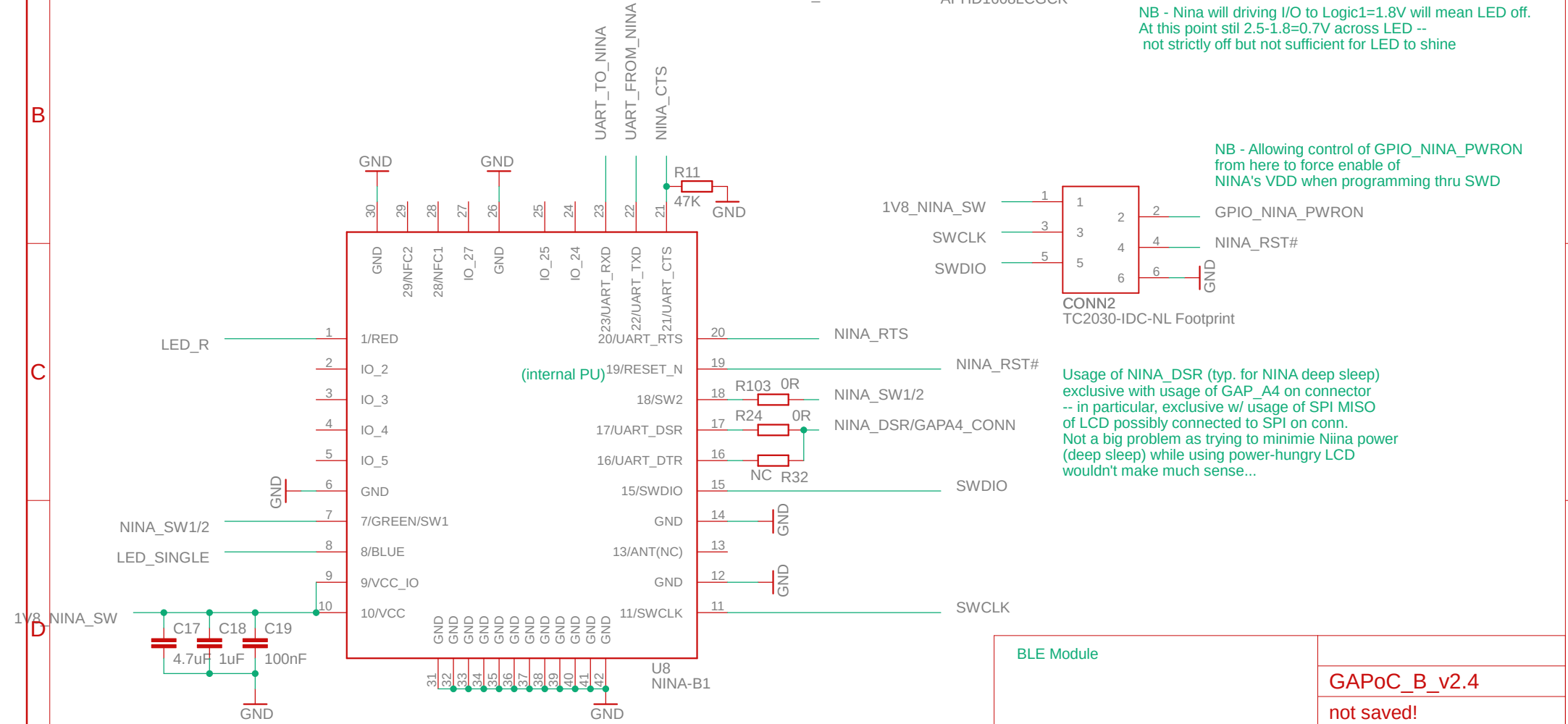


Switchable 2V5 (cf DIP Switch)
 Turn on for debug/bring-up,
 off to save power

2V5_LED



NB - Nina will driving I/O to Logic1=1.8V will mean LED off.
 At this point stil 2.5-1.8=0.7V across LED --
 not strictly off but not sufficient for LED to shine



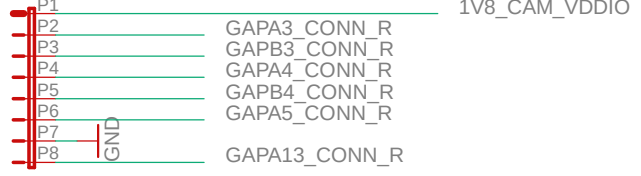
BLE Module

GAPoC_B_v2.4

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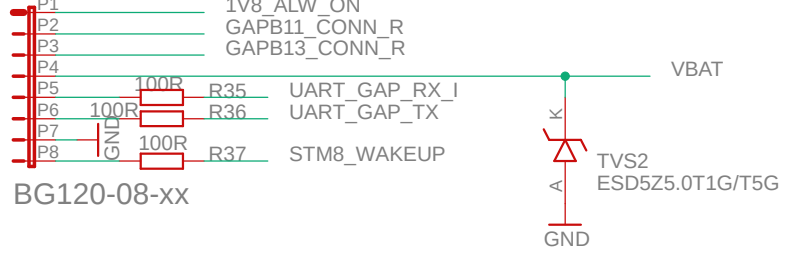
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CONN3

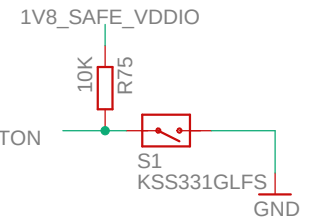


BG120-08-xx

CONN4

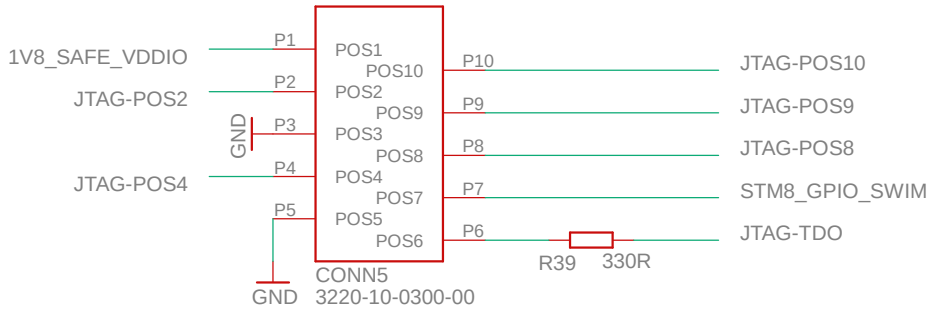


BG120-08-xx

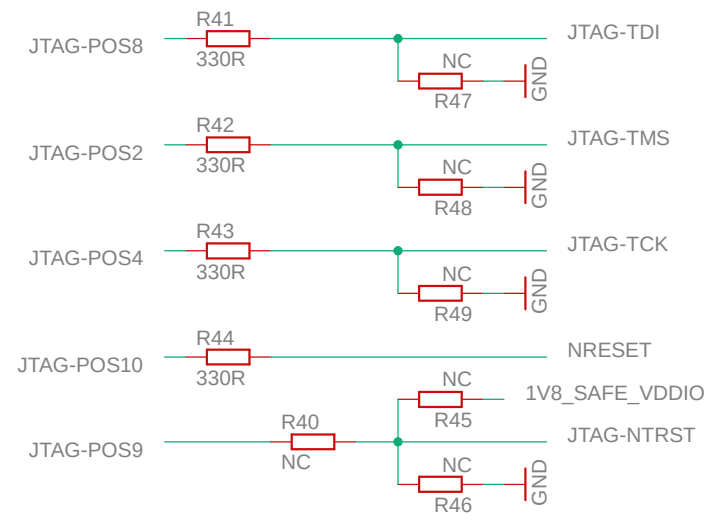


Push-button shares GAP_A13 with Conn3 Pos8

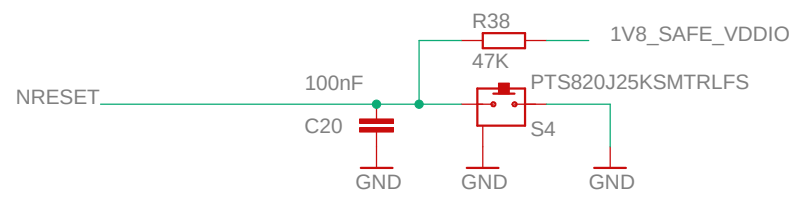
- SPIM1 on GAP_A4,B3,A5,B4
- I2C1 on B4, A5
- Timer/PWM on pins GAP_A13



JTAG Connector
 NOTE - This pinning is intended to be compatible with TagConnect TC2050 JTAG-ARM-20 to JTAG-ARM-10 converter and similar JTAG10 connectors



Pull resistors as back-up.
 Normally implemented on robe side.
 Series R on JTAG-NTRST to be NC or not depending on probe (or adapter) type



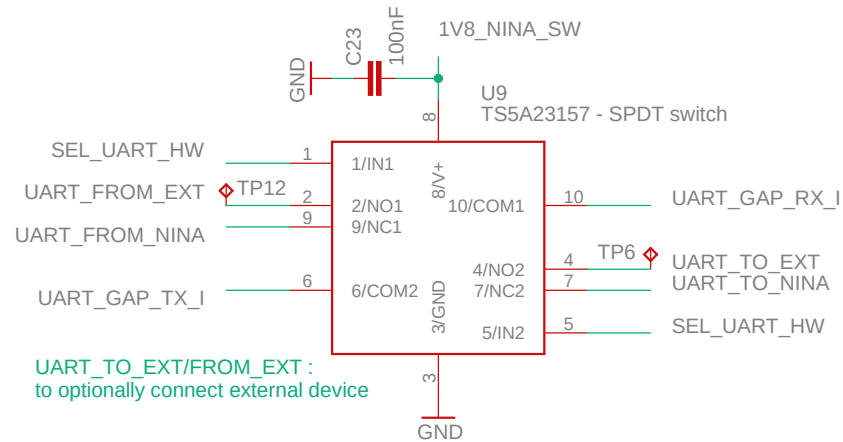
Connectors and Buttons

GAPoC_B_v2.4

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**** This could be optimized out ****
 Dropping UART_TO_EXT, UART_FROM_EXT.
 Keeping just UART for Nina (and CONN4)

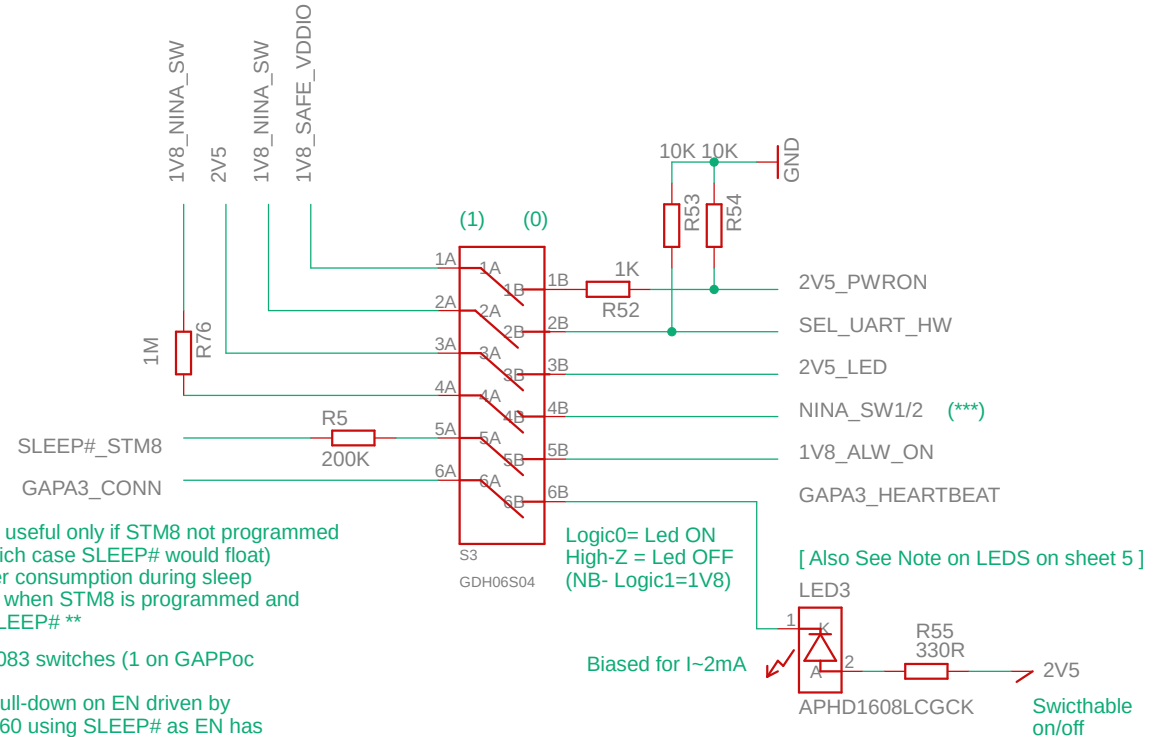


UART_TO_EXT/FROM_EXT :
 to optionally connect external device

Caution:
 when 1V8_Nina_Sw is switched off,
 GAP8 must drive UART_GAP_TX to Logic0
 to avoid excessive power consumption

Open/closed switches :

- 1: close to provide 2V5 to VQPS pin (Fuse prog.) and to on-board LEDs
- 2: select if GAP8's UART talks with NINA (open) or with external UART (closed)
- 3: close to enable status LEDs of NINA & IR sensor (which will draw a few mA)
- 4: close for normal boot of Nina
- 5: close to pull SLEEP# at start-up (required if STM8 not programmed), open to minimize static current
- 6: close to enable User LED, open to keep A3 available



Pull-up on SLEEP# useful only if STM8 not programmed / not present (in which case SLEEP# would float)
 Causes ~9uA power consumption during sleep
 ** Can be removed when STM8 is programmed and properly controls SLEEP# **

Beware - 2 MIC94083 switches (1 on GAPpoc and 1 on GAPMod) have weak (~2M) pull-down on EN driven by SLEEP# + TPS22960 using SLEEP# as EN has VIH=1.4V; therefore this pull-up can't be too weak.

Logic0= Led ON
 High-Z = Led OFF (NB- Logic1=1V8)
 [Also See Note on LEDS on sheet 5]
 LED3
 APHD1608LCGCK
 Biased for I~2mA
 2V5
 Swichable on/off

***** BEWARE: CLOSE position 4 of DIP switch for proper startup of Nina *****

NINA_SW12 pulled up selects normal boot.
 Using large R because same pin becomes LED_G output after startup (LED not implemented) -- which gets driven anyway by NINA hence current cons.
 Option to eliminate this extra power consumption by opening switch after startup.

***** BEWARE: CLOSE position 5 of DIP switch of STM8 not programmed / not placed *****
 Open once STM8 is programmed, to optimize system deep sleep current



Selection/configuration switches

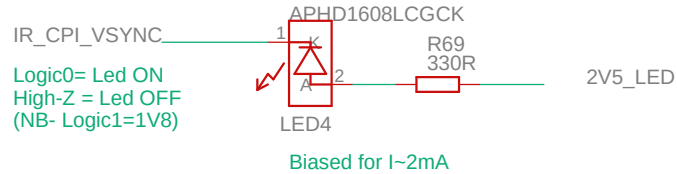
GAPoC_B_v2.4

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Status LED for IR Sensor Bring-up/Debug
Switch off 2V5_LED (cf DIP Switch) to save power when not required

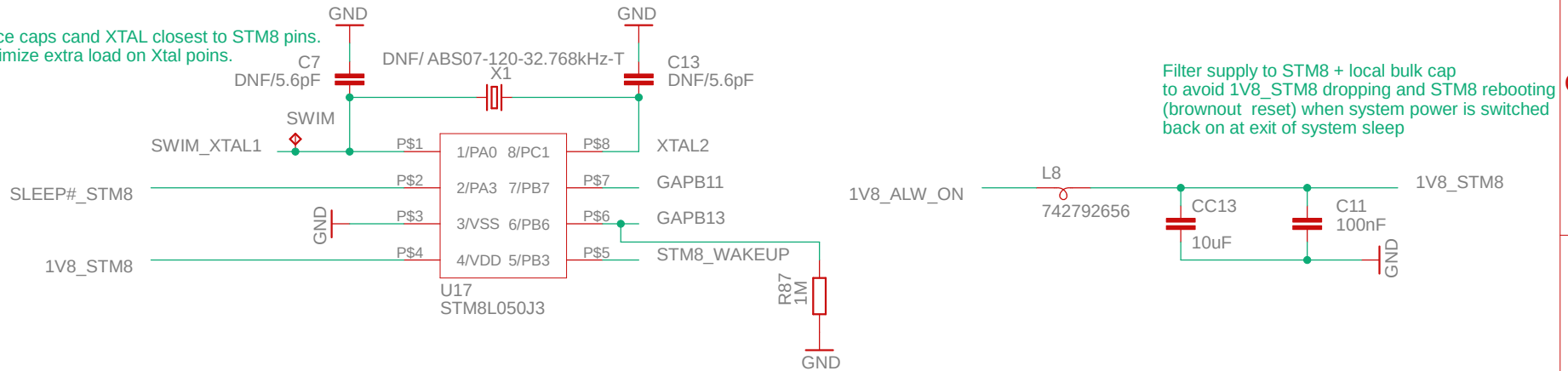
[Also See Note on LEDS on sheet 5]



[OPTIONAL -- this provides System DeepSleep/Watchdog + RTC functionality + helps getting to ultra-low system sleep power consumption
** Assembly Option **]

Xtal can be avoided if no RTC required, wake-up from external source only or if very approximate RTC (hence wake-up) period is acceptable.
STM8 Xtal required only if accurate system RTC functionality is required from STM8.
Else can use LSI of STM8 or just rely on wake-up from GPIO if RTC not needed.
If Xtal is implemented, SWIM must be disconnected from GAP8 after programming due to pin sharing on STM8.

Place caps and XTAL closest to STM8 pins.
Minimize extra load on Xtal pins.



Control of system sleep mode / WatchDog

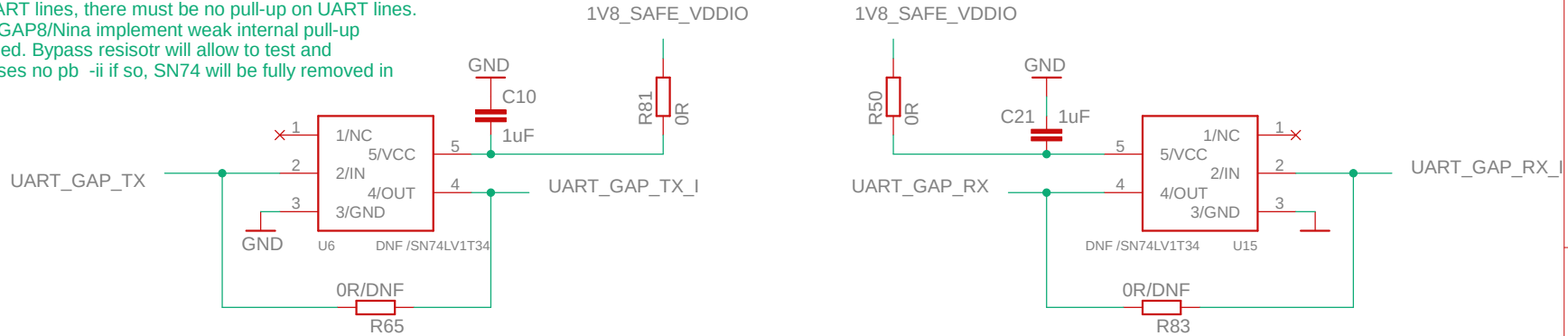
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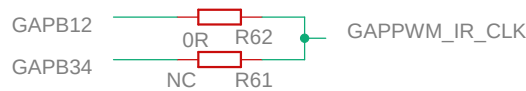
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**** Possible optimization ****

These 2 SN74LV1T34 were useful when Nina was on 3V. Since v2.2, Nina is on 1V8 so SN74 should be redundant. However, because GAPMod1.2 employs auto-bidir level shifters on UART lines, there must be no pull-up on UART lines. For now, still provision SN74, in case GAP8/Nina implement weak internal pull-up on UART I/Os that can't be fully disabled. Bypass resistor will allow to test and make 100% sure removing SN74 causes no pb -ii if so, SN74 will be fully removed in next revision.

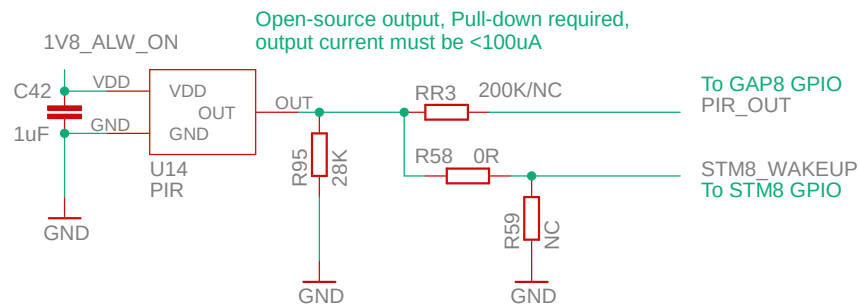


Both I/Os are Timer/PWM capable



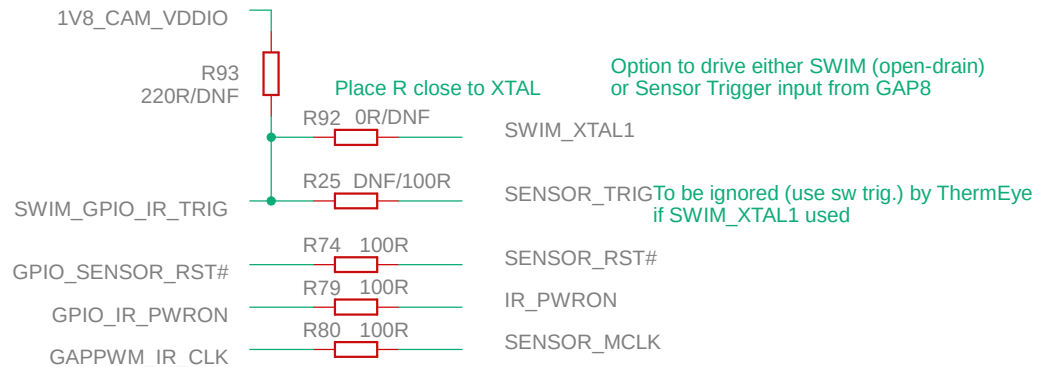
Padframe bug on B34 in CTu1.0/1.1 ==> don't use B34 as PWM, instead use GAPB12 as PWM_IR_CLK (however keep option to use B34 for when bug fixed as it allows to use IR sensor w/o 1V8 on)

PIR usable to Wake-up GAP8 or STM8



Open-source output, Pull-down required, output current must be <100uA

If RR3 implemented then PIR can also wake up GAP8 however in system deep sleep with GAP8 unpowered, will draw 9uA from PIR (if present)



Place R close to XTAL

Option to drive either SWIM (open-drain) or Sensor Trigger input from GAP8

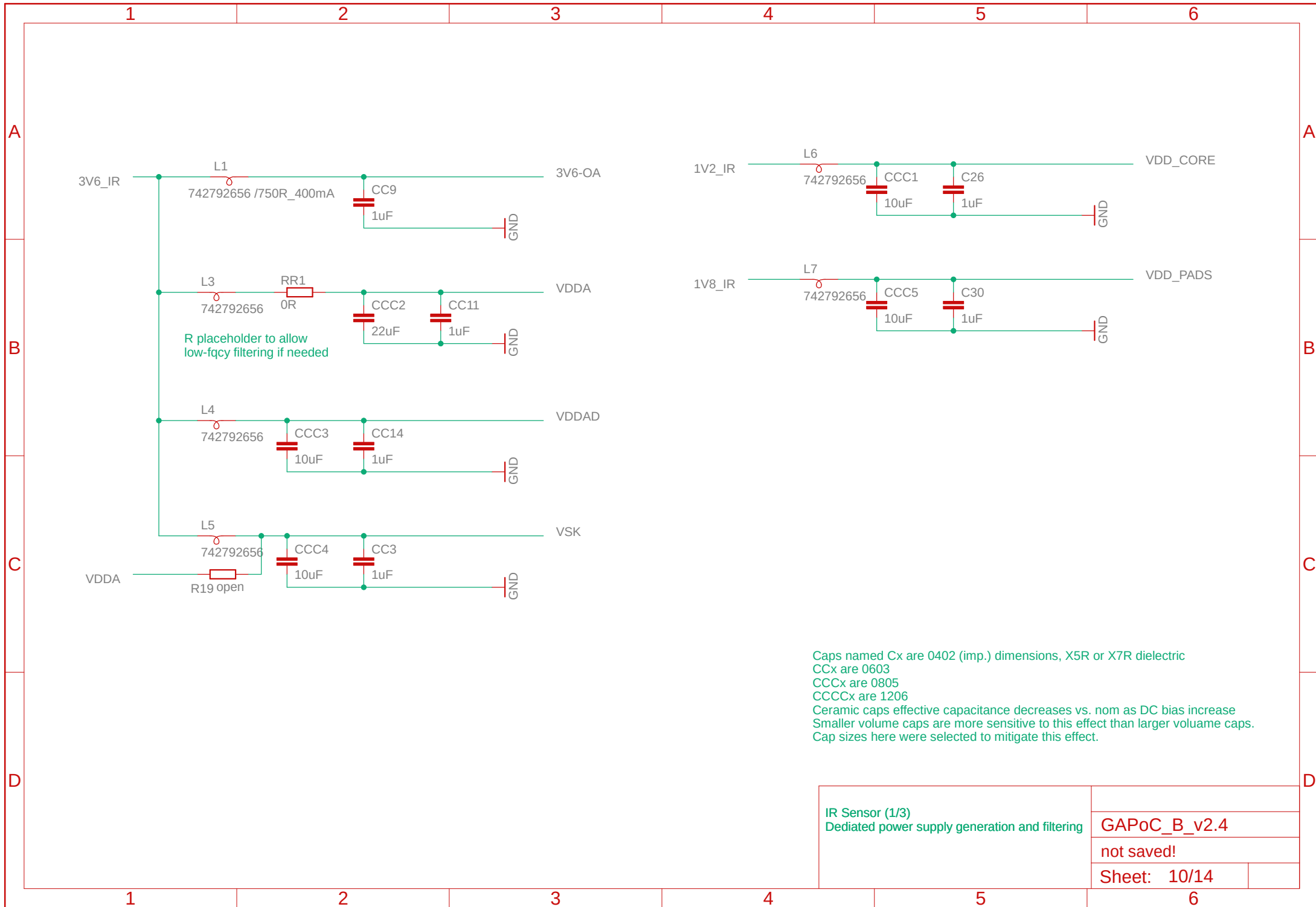
To be ignored (use sw trig.) by ThermEye if SWIM_XTAL1 used

Level Shifter & Misc.

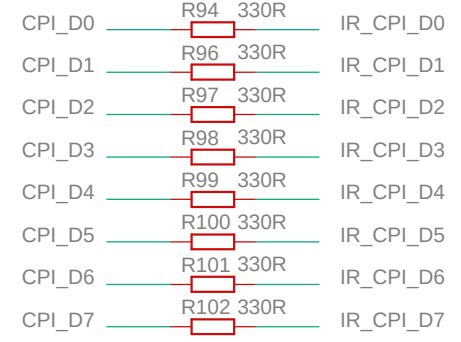
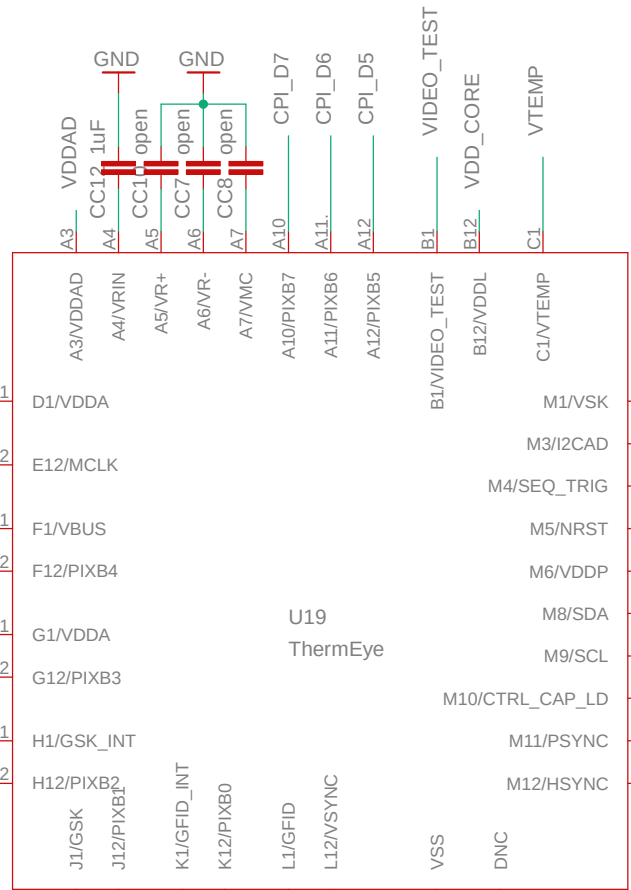
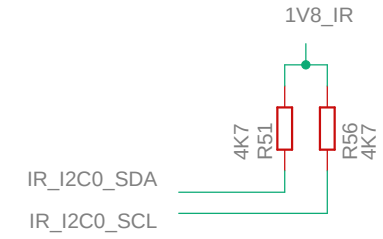
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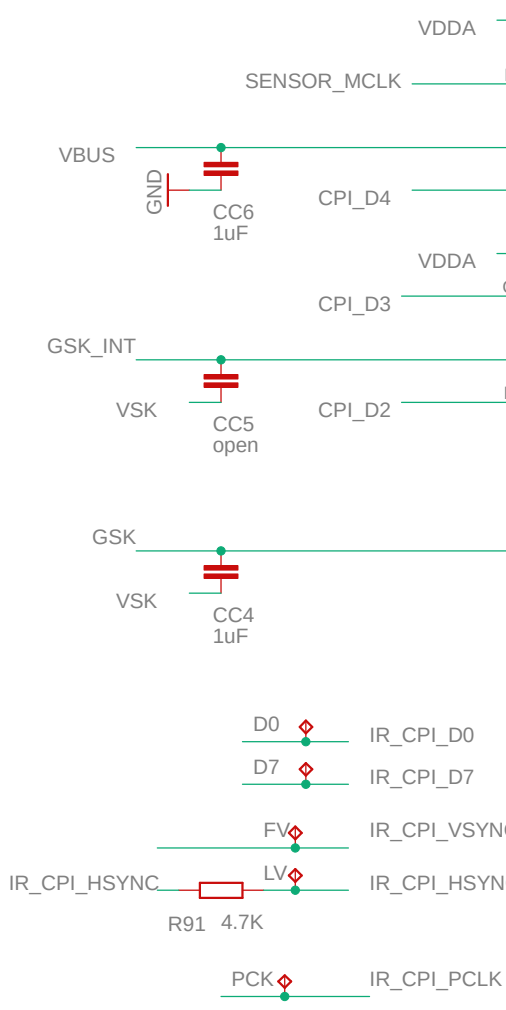
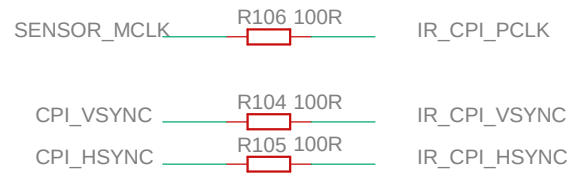
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Use 1V8_IR to pull I2C so that I2C pins of sensor don't get pulled when sensor is switched off



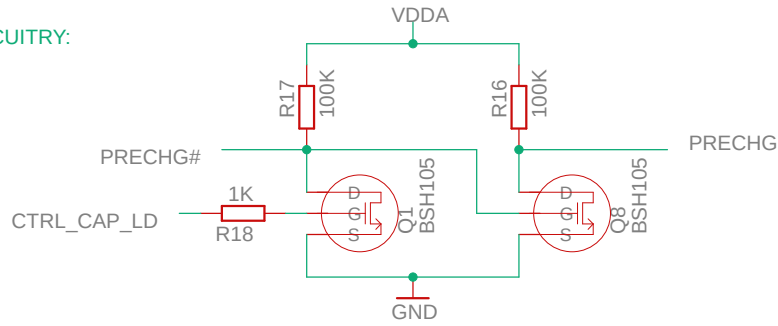
(* PSYNC is pixel (2 bytes) clock, we need byte clk (1 pixel is on 2 bytes) so rather take in MCLK as CPI clock



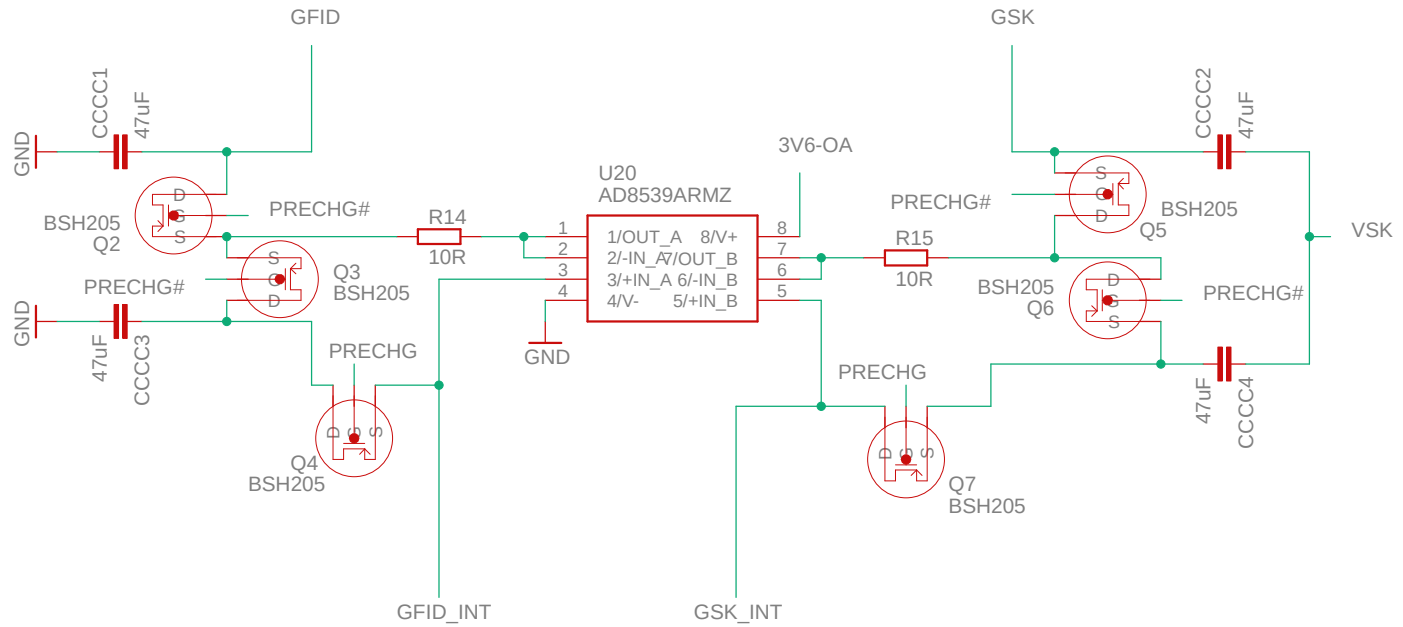
Bridge FV & LV on board to take *all* pixels of frame delimited by Vsync into CPI, incl. inter-line (Vsync 'wins' owing to series R, current = 1.8/4K7 ~ 360uA)

IR Sensor (2/3)
Sensor IC Connections and Level shifters

GENERATION OF PRECHARGE SIGNALS FOR BOOST CIRCUITRY:



GENERATION OF GFID AND GSK USING "TIME BOOST" :



IR Sensor (3/3)
Biasing with time boost

GAPoC_B_v2.4

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